CLAIMS

What is claimed is:

Claim 1. A method of manufacturing a structure, comprising the steps of:

forming shallow trench isolation (STI) in a substrate;

providing a first material on the substrate;

providing a second material on the substrate;

mixing the first material and the second material into the substrate by a thermal anneal process to form a first island and second island at a nFET region and a pFET region, respectively; and

forming a layer of material on the first island and the second island having a lattice constant different than the first island and the second island,

wherein the STI relaxes and facilitates the relaxation of the first island and the second island.

Claim 2. The method of claim 1, wherein the first material is deposited Ge material and the second material is deposited Si:C or C.

Claim 3. The method of claim 1, wherein the thermal anneal process takes place at about 1200 to 1350 C.

Claim 4. The method of claim 1, wherein the forming a layer of material step is growing a layer of Si material on the first island and the second island.

Claim 5. The method of claim 4, wherein the first island comprises substantially SiGe, the second island comprises substantially Si:C and the Si layer is a strained layer.

Claim 6. The method of claim 1, wherein the STI is formed of a material which has a lower viscosity as the temperature rises.

Claim 7. The method of claim 4, wherein the Si material is placed in a tensile stress on the first island and placed in a compressive stress on the second island.

Claim 8. The method of claim 1, wherein the first material is Ge with a Ge% of approximately less than 25% to the substrate.

Claim 9. The method of claim 1, wherein the first island and the second island have a different relaxed crystal lattice.

Claim 10. The method of claim 1, wherein the STI is a high temperature stable amorphous material.

Claim 11. The method of claim 1, wherein the first material and the second material are deposited on the substrate prior to the mixing step.

Claim 12. The method of claim 1, wherein the first material and the second material are grown on the substrate prior to the mixing step.

Claim 13. The method of claim 1, wherein the second material is implanted C at a dose which produces concentrations of greater than 1-2% Si:C upon the thermal anneal process.

Claim 14. The method of claim 1, wherein the layer of material includes selectively growing an Si epitaxial layer on the first island and the second island, the Si epitaxial layer having a different lattice constant than the first island and the second island such that the selectively grown Si epitaxial layer will strain tensilely and compressively on the first island and the second island, respectively.

Claim 15. The method of claim 1, wherein the first island has a lattice constant a ≥ aSi and the second island has a lattice constant a ≤ aSi.

Claim 16. The method of claim 15, wherein the first island is comprised substantially of SiGe and the second island is comprised substantially of Si:C and an epitaxially grown layer over the SiGe island and the Si:C layer is placed under a tensile stress and a compressive stress, respectively, by virtue of lattice matching of the epitaxially grown layer to the SiGe and Si:C.

Claim 17. The method of claim 1, wherein the second island is comprised substantially of Si:C and the C has a range of about 1-4% upon the thermal anneal process.

Claim 18. A method of manufacturing a semiconductor structure, comprising the steps of:

forming a substrate;

forming shallow trench isolation (STI) in the substrate with a first material;

providing a second material over a pFET region and an nFET region;

thermally annealing the first material into the substrate to form a first island and a second island of mixed material;

growing a Si layer on the first island in a first region, wherein the Si layer is strained.

Claim 19. The method of claim 18, wherein the second material is Ge and the first region is a pFET region and the Si layer becomes tensilely strained.

Claim 20. The method of claim 18, further comprising relaxing the STI and which facilitates relaxation of the first island and the second island during the thermally annealing step.

Claim 21. The method of claim 18, wherein the second material is Si:C or C and the first region is an nFET region.

Claim 22. The method of claim 21, wherein the Si layer becomes compressively strained.

Claim 23. The method of claim 18, wherein the thermal anneal step takes place at about 1200 to 1350 C.

Claim 24. The method of claim 18, wherein the first material has a lower viscosity as the temperature rises.

Claim 25. The method of claim 24, wherein the first material and the substrate are a high temperature stable amorphous material.

Claim 26. The method of claim 18, wherein the Si layer has a different lattice constant than the first island such that the Si layer will strain one of tensilely and compressively on the first island.

Claim 27. A method of manufacturing a semiconductor structure, comprising the steps of:

forming a substrate;

forming shallow trench isolation of high temperature stable amorphous material in the substrate;

thermally annealing at least one material into the substrate to form a first island and a second island of mixed material; and

growing an Si layer on at least the first island,

straining the Si layer in one of a compressive and tensile stress.

Claim 28. The method of claim 27, wherein the material is at least one of Ge and Si or Si:C.

Claim 29. The method of claim 27, wherein one of:

the at least one material is Ge and the first island and the second island is comprised substantially of a mixed material of relaxed SiGe,

the at least one material is C or Si:C and the first island and the second island is comprised substantially of a mixed material of relaxed Si:C, and

the at least one material is Ge and Si:C: or C and the first island is comprised substantially of SiGe and the second island is comprised substantially of Si:C.

Claim 30. The method of claim 29, wherein the Si layer is compressively strained when the mixed material is SiGe and tensilely strained when the mixed material is Si:C.

Claim 31. The method of claim 29, wherein the Si layer has a different lattice constant than the SiGe material and the Si:C material and the substrate is also formed from a high temperature stable amorphous material.

Claim 32. A semiconductor structure, comprising:

a substrate:

a relaxed shallow trench isolation of high temperature stable amorphous material formed in the substrate;

a first island of thermally annealed mixed material formed in the substrate at a pFET region;

a second island of thermally annealed mixed material formed in the substrate at an nFET region; and

a strained Si layer formed on at least one of the first island and the second island.

Claim 33. The structure of claim 32, wherein one of:

the first island and the second island is comprised substantially of a mixed material of relaxed SiGe,

the first island and the second island is comprised substantially of a mixed material of relaxed Si:C, and

the first island is comprised substantially of SiGe and the second island is comprised substantially of Si:C.

Claim 34. The structure of claim 33, wherein the high temperature stable amorphous material is Si which is compressively strained when the mixed material is SiGe and tensilely strained when the mixed material is Si:C.

Claim 35. The structure of claim 33, wherein the high temperature stable amorphous material has a different lattice constant than the first island and the second island.